Notice of Allowability	Application No.	Applicant(s)	
	10/725,593	SATO ET AL.	
	Examiner	Art Unit	
	MANSOUR M. SAID	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *5/26/06*.

2. ☒ The allowed claim(s) is/are *2-23 and renumbered as 1-22*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date ~~12/3/3~~ 12-03-03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Marquez, Juan Carlos on May 26, 2006.

2. The application has been amended as follows.

Please amend the claims as follows:

IN THE CLAIMS

Please cancel claim 1.

In claim 2, line 1, after "to claim" please delete "1" and insert --6 --.

In claim 5, line 1, after "to claim" please delete "1" and insert --6 --.

In claim 6, line 1, after "a display device" please delete "according to claim 1" and please add --having a level converting circuit including thin film transistors formed on a substrate, wherein the level converting circuit converts non-differential input signals having an amplitude of 1.2V or less into signals having a larger amplitude, wherein the input signals are control signals, --.

In claim 8, line 1, after "a display device" please delete "according to claim 1" and please add --having a level converting circuit including thin film transistors formed on a substrate, wherein the level converting circuit converts non-differential input signals having an amplitude of 1.2V or less into signals having a larger amplitude, wherein the input signals are display data, --.

(New) Claim 20, –A display device according to claim 8, wherein the input signals are signals which have an amplitude smaller than a twofold value of a threshold voltage of the thin film transistors. --.

(New) Claim 21, --A display device according to claim 20, wherein the input signals are signals which have an amplitude equal to or less than 1.6 times of a threshold voltage of the thin film transistors. --.

(New) Claim 22, -- A display device according to claim 20, wherein the input signals are signals are signals which have an amplitude equal to or more than a threshold voltage of the thin film transistors and equal to or less than 1.6 times of a threshold voltage of the thin film transistors. --.

(New) Claim 23, -- A display device according to claim 8, wherein the input signals are either control signals or display data. --.

Allowable Subject Matter

3. Claims 2-23 are allowed.

The following is an examiner's statement of reasons for allowance: Claims 2-23 are allowed since certain key features of the claimed invention are not taught or fairly suggested

by prior art. **In claims 6 and 14**, "a first-conductive-type first transistor which is connected between a first power source line to which a first voltage is supplied and an output terminal and has a gate electrode to which the input signals are applied through a first capacitive element; a second-conductive-type second transistor which is connected between the output terminal and a second power source line to which a second voltage is supplied and has a gate electrode to which the input signals are applied through a second capacitive element; a first bias circuit which applies a first bias voltage to the gate electrode of the first transistor; and a second bias circuit which applies a second bias voltage to the gate electrode of the second transistor". **In claims 8 and 16**, "a first switching element having a first electrode which is connected to a first power source line to which a first voltage is supplied; a second switching element having a second electrode which is connected to a second electrode of the first switching element and a first electrode which is connected to the second electrode of the transistor, and a bias circuit applying a bias voltage to a first electrode of the transistor, wherein the bias voltage is a voltage which turns off the transistor when a voltage applied to a gate electrode of the transistor assumes a minimum value ". **In claim 10**, a first-conductive-type first transistor which is connected between a first power source line to which a first voltage is supplied and an output terminal and has a gate electrode to which the control signals are applied through a first capacitive element; a second-conductive-type second transistor which is connected between the output terminal and a second power source line to which a second voltage is supplied and has a gate electrode to which control signals are applied through a second capacitive element, and a third transistor having a gate electrode to which an output voltage of the sample holding circuit is applied; a first switching element having a first electrode which is connected to the first power source line; a

second switching element having a second electrode which is connected to a second electrode of the first switching element and a first electrode which is connected to a second electrode of the third transistor. The closest prior art Maekawa et al. (5,748,026) teaches a level converting circuit for an input clock signal having a relatively low amplitude, and a level converting circuit for converting the input click signal to an output click signal having a relatively high amplitude, the level converting circuit having an input transistor which has a predetermined threshold voltage, and detecting/offsetting circuit for detecting the threshold voltage of the input transistor; Haga (7,006,068 B2) teaches a sampling level converter circuit includes first to third transistors connected serially between a higher potential power-supply and a lower-potential power-supply, a first capacitor connected to a connection node of the first and second transistors; Miyazawa Toshio (2002251174 A) teaches a voltage level converter comprising input terminal connected to capacitors and gates of NMISTFT1 & PMISTFT1, and the second terminal are connected respectively to a low voltage supply side and the connection point of the second terminal of the PMISTFT3 and the first terminal of the NMISTFT3 are made to be an output terminal, however, singularly or in combination with other prior art, fail to anticipate or render the above underlined limitations obvious.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Orisaka et al. (6,107,857) teach a level converting circuit converts the level of an input signal to a positive or a negative level according to a power source voltage for supplying a voltage of a reference level for the input signal.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mansour M. Said whose telephone number is 571-272-7679. The examiner can normally be reached on Monday through Thursday from 8:30-6:00 P.M. The examiner can also be reached on alternate Friday from 8:30 a.m. to 5:00 p.m. EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hjerpe, Richard A. whose telephone number is 571-272-7691.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: 571-273-8300 (for Technology Center 2600 only)

Hand-delivered responses should be brought to the Customer Service Window at the Randolph Building, 401, Dulany Street, Alexandria, VA 22314.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mansour M. Said

5/26/06

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